



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,902	08/21/2003	Cheng-Ming Yih	4425-315	6430

7590 05/16/2005

LOWE HAUPTMAN GILMAN & BERNER, LLP
Suite 310
1700 Diagonal Road
Alexandria, VA 22314

EXAMINER

HO, TU TU V

ART UNIT	PAPER NUMBER
----------	--------------

2818

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action

Application No.

10/644,902

Applicant(s)

YIH ET AL.

Examiner

Tu-Tu Ho

Art Unit

2818

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 21 April 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
- b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
- ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
- (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
- (b) ☐ they raise the issue of new matter (see Note below);
- (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
- (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____


3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☒ Newly proposed or amended claim(s) 21-24; however, see note in section (10, II) below would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☐ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.


The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: 21-24; however, see note in section (10, II) below.Claim(s) objected to: 11.Claim(s) rejected: 1-13.

Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____.
10. ☒ Other: See Continuation Sheet


David Nelms
Supervisory Patent Examiner
Technology Center 2800


Tu-Tu Ho 05/02/2005

(I) of the reasons stated in the last Office Action (paper mailed 01/21/2005) concerning claims 1-13. Specifically:

Song's buried conductive region 113a is indeed under the isolation regions (105) as argued by Applicant, but is also **between** the isolation regions).

This cross-sectional view shows a series of gates (107) and a data line (108) on a substrate (100). The gates are separated by spacers (113a) and have a top layer (114). The data line is on top of the gates and has a top layer (115). The gates are connected to a word line (WL) (109). The data line is connected to a bit line (BL) (116). The gates are labeled 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200.

As for the limitation “a depth of said buried source line is less than a depth of said plurality of isolation regions” as argued by Applicant, the limitation is not in the pertinent claims.

(2) In re the Lee reference, Applicant correctly argued that Lee's "[E]ach source array has a plurality of source regions 124 separately positioned between device isolation lines 102".

Art Unit: 2818

Therefore, if Lee's source region 124 is equivalent to the claimed buried **conductive region** (240), which is the case, and if Lee's device isolation lines 102 are equivalent to the claimed isolation regions (210), which is also the case, then Lee's buried conductive region 124 is separately positioned between device isolation regions 102, or in other words, a buried conductive region (124) between said plurality of isolation regions (102).

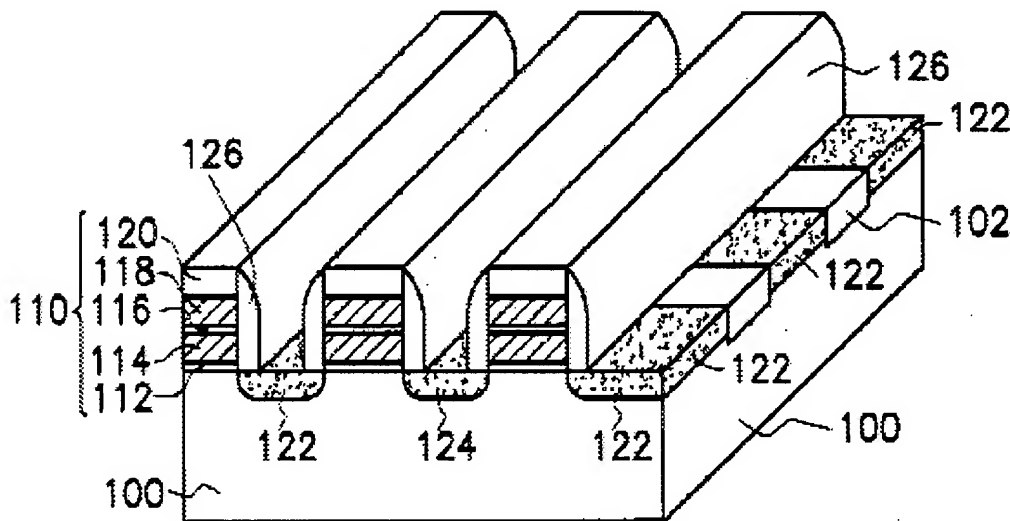



FIG. 2C

As for the argument that the depth of the source region can not be visually compared with that of the isolation region, since the depth of the source region (124) can be visually compared with that of the drain region (122, which as clearly depicted from Fig. 2C has a depth similar to that of source region 124 – reinforced by the general knowledge in the art that a source region and a drain region of a nonvolatile memory device have the same depth, which is the case of the Lee's reference, unless specifically formed differently, which is not the case with the Lee's reference) and since the depth of the drain region can be visually compared with that of the isolation region, the depth of the source region can be visually compared with that of the isolation region.

(II) The dependencies of claims 22-24 are defective because claim 14 was canceled.


 David Nelms
 Supervisory Patent Examiner
 Technology Center 2800